REMARKS

Claims 2, 3, 4, 5, 6, 8, 9, 11, 16, 17, 18, 20, 23, 44 - 47, 53, 54, 56 - 59 are pending.

Objections

Claim 16 is amended to correct a mere informality as suggested by the Examiner.

Claim rejection 35 USC 102(b)

Claims 3-6, 8, 9, 17, 18, 20, 44, 46, 47, 53, 54, and 56-58 are rejected under Tanioka.

Tanioka

The Office Action alleges that Tanioka discloses an unpackaged semiconductor die 2, (FIGS. 2A-2C) directly attached to the package module, the unpackaged semiconductor die encapsulated 16, (FIG. 2A), onto the package module in a structure having a planar top surface. Applicants submit that, Tanioka is directed to a multi chip module having wiring layers on front and back surfaces. (Col. 3, lines 54 – 57). A carrier board 3 disposed at the back surface of the multi chip module includes pads for external connection. (Col. 3, line 67 – Col. 4, line 11). By changing the pad arrangement to a matrix arrangement, the spacing between the external connection terminals reduces solder flowing between pads, thus increasing yield. (Col. 5, lines 33-37). A silicon layer 9 is interposed between the MCM board 1 and the carrier board 3 to enable cooling of the bare chip. (Col. 5, lines 9-10; Col. 5, lines 41-43).

Independent Claim 56

Independent claim 56 recites, among other features, ... an ... unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and a packaged semiconductor die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

Firstly, Applicants submit that Tanioka is wholly different than Applicants' claimed subject matter as Tanioka adds a carrier board 3 to the multi chip module 1 rather than to position the encapsulation structure in a coplanar fashion relative to the top portion of a neighboring package module. Applicants submit that the encapsulation design of Tanioka lacks the advantages present in Applicants' claimed subject matter. For example, Applicants' planar top surface of an encapsulation structure which is positioned in a coplanar fashion relative to the top portion of a neighboring package module, such that a heat sink having a planar bottom (e.g., a simple universal design), can be placed on top of both the top surface of the encapsulation structure and on the top portion of a neighboring package module. As a result, the heat sink in this configuration is in contact with both items and rests upon a relatively large portion of both items where the large contact, between both the encapsulation structure and the neighboring package module and the heat sink, allow for significant heat transfer from both items to the heat sink. In contrast, the encapsulation design disclosed in Tanioka is less desirable than Applicants' claimed subject matter because, rather than dissipate heat with a heat sink, Tanioka applies a silicon layer to enable cooling of the bare chip. Further when a heat sink, having a planar surface, is placed on top of both the packaged and encapsulated semiconductor dies having different heights, such heat sink then assumes an angled position across the two items. In such a position, the heat sink only contacts the edge of the packaged heat sink and only a point of the dome, i.e., as shown in FIGS. 1, 3 in Tanioka of the encapsulated material. As such, the resulting heat transference is relatively small and the physical connection to the heat sink is positioned on an undesirable angle resulting in a number of disadvantages. It should be also noted that, regardless of the height of the top surface of the domed shaped encapsulated structure, any heat sink with a planar surface in contact with devices of different heights only

shares a small contact position therewith, and as such, will result in a relatively poor transference of heat there between.

Secondly, since Tanioka teaches a silicon layer 9 interposed between the MCM board 1 and the carrier board 3 to enable cooling of the bare chip, Tanioka teaches away from contacting a coplanar heat sink surface and therefore teaches away from a planar top surface of an encapsulation structure positioned in a coplanar fashion with the neighboring package module. Since Tanioka teaches a totally different and less effective form of heat dissipation, the solution taught by Tanioka is unsatisfactory and therefore teaches away from the claims. Applicants submit that the encapsulation design of Tanioka lacks these and other advantages present in Applicants' claimed subject matter. Another example of such an advantage includes the fact that Applicants' metal cap encapsulation technique provides the advantages associated with the properties of metallic structures generally, and more specifically, for some embodiments, the presence of a gap between the enclosed die and surrounding metal cap structure itself. In contrast, the silicon layer 9 interposed between the carrier board 3 and the MCM board 1 as taught by Tanioka is less desirable than Applicants' claimed subject matter as such material is not metal and therefore does not provide the metallic properties such as heat transfer provided by Applicants' claimed subject matter, nor is such material a metal cap as acknowledged in the Office Action.

Thirdly, Applicants submit that nowhere in the Office Action does the Examiner specifically point out where the references recite the claim limitation "wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." Because Applicants can identify no language in Tanioka as cited that makes reference to the height of the packages, and because Tanioka teaches

mounting a carrier board 3 directly to the package modules rather than a heat sink, and further because FIG. 2 as cited shows the small outline package 17 shown rises to a height that is less than the height of a neighboring package module 2, Applicants submit that Tanioka does not disclose Applicants' claimed subject matter, but further teaches against Applicants' invention. As such, it is respectfully submitted that claim 56 is allowable as written.

The Office Action asserts that FIGS. 2A-2C of Tanioka describe the elements of Claim 1. Firstly, according to FIG. 2A in Tanioka, the chip part 7 is shown rise to a height that is less than the height of a neighboring structure molded by a protective resin 16. Similarly, small outline package 17 is shown rise to a height that is less than the height of a neighboring package module 2. This is unlike Applicants' claimed subject matter having, inter alia, an "encapsulated ... structure having a planar top surface ... wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate. (claim 56).

Applicants submit that Tanioka does not disclose, teach or suggest claim 56's language including, inter alia, "...an ... unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and a packaged semiconductor die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." Nor does Tanioka disclose, teach or suggest the subject matter of claim 56 as a whole. Applicants submit that at least for the reasons that Tanioka discloses an encapsulated structure covered by a carrier board 3 where such structure is shown as being located at a position having a height different than of a neighboring package module, that independent claim 56 is neither anticipated, nor is obvious in view of Tanioka.

Independent Claim 57

Independent claim 57 recites, among other features, ... a ... graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate.

Applicants respectfully reassert the arguments made above regarding Tanioka. Further, Applicants submit that, Tanioka does not disclose, teach or suggest, claim 57's language including, inter alia, "...a ... graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate.," nor does Tanioka disclose, teach or suggest the subject matter of claim 57 as a whole. Applicants submit that at least for the reasons that Tanioka discloses an encapsulated structure covered by a carrier board 3 where such structure is shown as being located at a position having a height different than of a neighboring package module, that independent claim 57 is neither anticipated, nor is obvious in view of Tanioka.

The Office Action asserts that the semiconductor module "sized to be interchangeable with standard package sizes" employs intended use language. Nevertheless, the claim language "a package module sized to be interchangeable with standard package sizes" (see M.P.E.P. 2173(b)) is sufficiently accurate, and therefore, the rejection is improper[1].

[1] Orthokinetics, Inc. v. Safety Travel Chairs, Inc., 806 F.2d 1565, 1 USPQ2d 1081 (Fed. Cir. 1986), *see also* M.P.E.P. 2173.05(b).

Independent Claim 58

Independent claim 58 recites, among other features, an unpackaged semiconductor die ... encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

Applicants respectfully reassert the arguments made above regarding Tanioka. Further, Applicants submit that, Tanioka does not disclose, teach or suggest, claim 58's language including, inter alia, "...an unpackaged semiconductor die ... encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.," nor does Tanioka disclose, teach or suggest the subject matter of claim 58 as a whole. Applicants submit that at least for the reasons that Tanioka as cited discloses an encapsulated structure covered by a carrier board 3 where such structure is shown as being located at a position having a height different than of a neighboring package module. Therefore, that independent claim 58 is neither anticipated, nor is obvious in view of Tanioka.

Dependent Claims 3 and 4

Applicants respectfully reassert the arguments made above regarding claim 56. In addition, Applicants also submit that because claims 3 and 4 depend from claim 56, and as a dependent claim therefrom, claims 3 and 4 are allowable for at least the reasons claim 56 is allowable. As acknowledged in the Office Action, nowhere does Tanioka disclose, teach or suggest wherein the unpackaged semiconductor die is a graphics-processor, or where the

packaged semiconductor is a memory. As such, Tanioka does not disclose, teach or suggest Applicants' claimed subject matter. Applicants further submit, argued in part at least immediately above, that claims 3 and 4 are also allowable in light of the presence of novel and non-obvious elements contained in claims 3 and 4 that are not otherwise present in claim 56. Additionally, pursuant to M.P.E.P. 2144.03, Applicants respectfully challenge the assertion that Tanioka "encompasses all well known semiconductor die's including a 'memory die'" as asserted with respect to claims 3 and 4 and requests that supporting reference be cited for each element of these claims if the rejection is maintained.

Dependent Claims 5 and 6

Applicants respectfully reassert the arguments made above regarding claim 56. In addition, Applicants also submit that because claims 5 and 6 depend from claim 56, and as a dependent claim there from, claims 5 and 6 are allowable for at least the reasons claim 56 is allowable. Applicants further submit, argued in part at least immediate above, that claims 5 and 6 are also allowable in light of the presence of novel and non-obvious elements contained in claims 5 and 6 that are not otherwise present in claim 56.

Dependent Claims 8 and 20

Applicants respectfully reassert the arguments made above regarding claims 56 and 57 respectively. In addition, Applicants also submit that because claims 8 and 20 depend from claims 56 and 57 respectively, and as a dependent claim therefrom, claims 8 and 20 are allowable for at least the reasons claims 56 and 57 are allowable. Applicants further submit, argued in part at least immediate above, that claims 8 and 20 are also allowable in light of the presence of novel and non-obvious elements contained in claims 8 and 20 that are not otherwise present in claims 56 and 57. Although the Examiner asserts that the burden of proof is on the

Applicants, the burden of proof for establishing a *prima facie* case of anticipation and obviousness rests on the Examiner, not on the Applicants.[2] Since the Examiner has not established a *prima facie* case of anticipation or obviousness, the rejections are improper.

Dependent Claim 9

Applicants submit that Tanioka does not disclose, teach or suggest, either explicitly or implicitly, Applicants claimed, inter alia, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die. (Claim 9). In contrast, FIG. 2C in Tanioka shows the opposite situation, where the small outline package 17 has a foot print that is greater than the footprint of the bar chip 2. Applicants assume that the Office Action's reference to the encapsulated structure 2 is a typographical error and actually refers to element 17 and visa versa as previously asserted with respect to claim 56. As such, Applicants respectfully submit that Tanioka does not disclose, teach or suggest Applicants claimed subject matter of claim 9.

Dependent Claims 17 and 18

Applicants respectfully reassert the arguments made above regarding claim 57. In addition, Applicants also submit that because claims 17 and 18 depend from claim 57 and, therefore, dependent claims 17 and 18 are allowable for at least the reasons claim 57 is allowable. Applicants further submit, argued in part at least immediate above, that claims 17 and 18 are also allowable in light of the presence of novel and non-obvious elements contained in claims 17 and 18 that are not otherwise present in claim 57.

[2] See M.P.E.P. §2142 and case citations therein.

Dependent Claims 44, 45, 46, 47, 53 and 54

Applicants respectfully reassert the arguments made above regarding claim 58. In addition, Applicants also submit that because claims 44, 45, 46, 47, 53, and 54 depend from claim 58, and, therefore, dependent claims 44, 45, 46, 47, 53, and 54 are allowable for at least the reasons claim 58 is allowable. Applicants further submit, argued in part at least immediate above, that claims 44, 45, 46, 47, 53, and 54 are also allowable in light of the presence of novel and non-obvious elements contained in claims 44, 45, 46, 47, 53, and 54 that are not otherwise present in claim 58.

Claim rejection 35 USC 103

Claims 2, 16, and 45

Claims 2, 16, and 45 are rejected under 35 U.S.C. 103(a) under Tanioka in view of Fallon et al.

Applicants submit that there must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify the references as described in order to produce the claimed invention[3]. First, as stated above, Tanioka teaches away from the claims because among other things, Tanioka teaches mounting a carrier board 3 directly to the package modules rather than a heat sink, and therefore Tanioka teaches away from "wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." As stated in the response to the Office Action dated January 1, 2003, Fallon teaches an encapsulation material as only having an arc, or dome shape and therefore also teaches against "wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." Since both Tanioka and Fallon

teach against the claims, there is no motivation to combine the references to produce the claimed invention[4]. Without the presence of any such motivation to combine such references to produce Applicant's invention, the later suggestion to combine such references is impermissible hindsight, and as such, is an invalid argument for a finding of unpatentability due to obviousness.

Claims 11 and 23

Claims 11 and 23 are rejected under 35 U.S.C. 103(a) under Tanioka in view of Takano et al. However, no reference to a patent number could be found in the Office Actions referring to Takano, and further, no reference to a patent to Takano could be found in the attached PTO-892 form entitled "Notice of References Cited." Accordingly, if this rejection is maintained, a citation to the Takano reference is respectfully requested. As such, Applicants cannot respond to this rejection, at least to the extent Takano is cited, and therefore such a rejection should be considered as a new rejection if the rejection is maintained.

Applicants respectfully reassert the arguments made above regarding claims 56 and 57. In addition, Applicants also submit that because claims 11 and 23 depend from claims 56 and 57 respectively, and as a dependent claim there from, claims 11 and 23 are allowable for at least the reasons claims 56 and 57 are allowable. Applicants further submit, argued in part at least immediate above, that claims 11 and 23 are also allowable in light of the presence of novel and non-obvious elements contained in claims 11 and 23 that are not otherwise present in claims 56 and 57

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[3] In re Fritch, 922 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). See M.P.E.P. §2143.03.
[4] A prior art reference must be considered in its entirety, i.e. as a whole including portions that would lead away from the claimed invention. (W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 U.S.P.Q 303 (Fed. Cir. 1983). See M.P.E.P. §2141.02.

Independent Claim 59

Claim 59 is rejected under 35 U.S.C. 103(a) under Tanioka in view of Distefano. Independent claim 59 recites, among other features, an unpackaged semiconductor die ... encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap. Applicants submit that neither Tanioka nor Distefano either in combination nor individually disclose, teach or suggest, claim 59's language including, inter alia, "...an unpackaged semiconductor die ... encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap." Further, Tanioka and Distefano either in combination or individually fail to disclose, teach or suggest the subject matter of claim 59 as a whole.

The Office Action acknowledges that "Tanioka does not disclose the encapsulating structure being further comprised of an encapsulating material of a metal cap." Secondly, Distefano as cited requires that the cap 20 include "a pair of flanges 26 projecting outwardly from flanges 24 at the forward edges thereof, remote from rear wall 22." Such flanges on the metal cap of the encapsulating material would impermissibly interfere with the unpackaged semiconductor and therefore increase the surface area of the module. As a result, the suggestion to modify Tanioka with Distefano would impermissibly change the principal of operation of Tanioka. Accordingly, since the proposed modification or combination of the Tanioka reference would change the principle of operation of Tanioka, the teachings of the reference are not

sufficient to render the claims *prima facie* obvious.[5] Applicants submit that at least for the reasons above that the combination of Tanioka and Distefano are improper and, therefore, the Office Action fails to establish a *prima facie* case of obviousness for independent claim 59.

Applicants respectfully submit that the claims are in condition for allowance. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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[5] In re Gordon, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984), *also see* M.P.E.P. 2143.01, "The Proposed Modification Cannot Change the Principle of Operation of a Reference".